REMARKS

Claims 34-42 are in the application. Claims 1-33 have been cancelled.

By this amendment, applicants have added new claims 34-41. Cancelled claim 1, applicants' specification including paragraphs [0013], [0017], [0020], [0023], [0026], and [0027], and FIGS. 4-6 support new claim 34. Paragraph [0020] supports new claim 35. Cancelled claim 8 and FIG. 4 supports new claim 36. Cancelled claim 9 supports new claim 37. Cancelled claim 6 supports new claim 38. Paragraph [0026] supports new claims 39-41. Paragraph 17 supports new claim 42.

New claim 34 calls for an intermediary of a semiconductor device comprising a semiconductor substrate formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate. A pillar region comprising a dielectric material is formed in the first recessed region and extends from the lower surface, wherein a void region is formed within the pillar region. A polysilicon cap layer is formed overlying upper surfaces of the pillar region and adjacent the void region, wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Applicants respectfully submit that claim 34 is allowable over the prior art of record including Akatsu et

al. (USP 6,333274), Lur et al. (USP 5,640,041), Davies (USP 6,512,283), Kadosh et al. (USP 6,069,398), Zekeriya et al. (US Publication 2003/0030107), and Holbrook et al. (USP 6,495,853) because none of the references, either singularly or in combination teach or suggest:

1. a pillar region comprising a dielectric material formed in a first recessed region and extending from the lower surface;
2. a void region formed within the pillar region; and
3. a polysilicon cap layer formed overlying upper surfaces of the pillar region and adjacent the void region, wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Claims 35-42 depend from claim 34 and are believed allowable for at least the same reasons as claim 34.

With the cancellation of claims 1-33, applicants respectfully believe that no fee is due for new claims 34-42. However, applicants hereby authorize the Commissioner to charge any fees due or refund any amounts due, to Deposit Account 501086.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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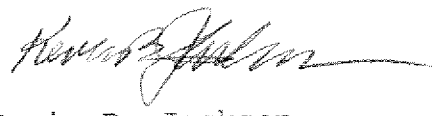

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